Doc. Ref.: AO54

## PATENT ABSTRACTS OF JAPAN

(11)Publication number:

04-123614

(43) Date of publication of application: 23.04.1992

(51)Int.CI.

H03K 19/0175

(21) Application number: 02-245491

(71)Applicant : NEC CORP

(22)Date of filing:

**14.09.1990** (72)Inve

(72)Inventor: YAMAZAKI TORU

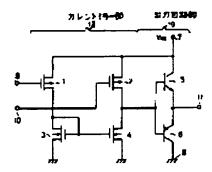
**SUGIYAMA MITSUHIRO** 

## (54) LEVEL CONVERTING CIRCUIT

## (57)Abstract:

PURPOSE: To remarkably decrease the number of elements and to improve the signal propagation speed by constituting an output circuit part of a series circuit of an NPN bipolar transistor and a PNP bipolar transistor.

CONSTITUTION: When a high level and a low level are inputted to an input terminal 9 and an input terminal 10, respectively, a P channel MOS transistor 1 becomes a turn-off state, and an N channel MOS transistor 4 for allowing a mirror output current to flow becomes a turn-off state. On the other hand, a P channel MOS transistor 2 through which a mirror output current flows comes to a turn-on state, a base current of an NPN bipolar transistor 5 is supplied and comes to a turn-on state, and an output terminal 11 goes to a high level. Subsequently, when a low level and a high level are inputted to the input terminal 9 and the input terminal 10, respectively, the P channel MOS transistor 1 comes to a turn-on state, and the N channel MOS transistor 4 and a PNP bipolar transistor 6 come to a turn-on state, therefore, the output terminal 11 goes to a low level.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of

rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2000 Japan Patent Office